ABSTRACT

A Low K dielectric layer (20) is formed over a semiconductor (10). Trenches (110, 120) are formed in the dielectric layer (2) and a barrier layer (70) is formed in the trenches. The barrier layer has a thickness of X_1 over the upper surface of the dielectric layer and X_2 on the sidewalls of the trenches where X_1 is greater than X_2. A second barrier layer (130) can be formed over the first barrier layer (70) and copper (100) is formed over both barrier layers to fill the trench.